UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,734	12/30/2003	Yibin Ye	110350-134110	9041

31817 7590 02/10/2006

SCHWABE, WILLIAMSON & WYATT
PACWEST CENTER, SUITE 1900
1211 S.W. FIFTH AVE.
PORTLAND, OR 97204

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,734	YE ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,11,12,14-17 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11,12,14-17 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 01/12/2006 has been entered.

2. Claims 1-3,11-12,14-17,21-23 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-3,11-12,14-17,21-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 14-17 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the contents in claims 14-17.

Regarding claims 14-17, these claims are depended from claim 13. However, applicant canceled claim 13.

These claims must be canceled or amended are requested.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Oikawa (U.S. Patent No. 5,675,160).

Regarding claim 1, Oikawa discloses a two-transistor DRAM cell (Figure 4) consisting:

an NMOS device (N1) with a first gate;

a PMOS device (P2) with a second gate, the PMOS device coupled to the NMOS device (Figure 4, N1 device coupled second gate of P2 device at n2) ; and

a storage node coupled to the second gate (Figure 4, n2) .

Regarding claim 21, Oikawa discloses a system (Figure 4) comprising:

an integrated circuit (IC) (Column 1, lines 6-10); and

memory (Figure 4) coupled to the IC, the memory including at least one two-transistor DRAM cell consisting:

an NMOS device (N1) with a first gate;

a PMOS device (P2) with a second gate, the PMOS device coupled to the NMOS device (Figure 4, N1 device coupled second gate of P2 device at n2) ; and

a storage node coupled to the second gate (Figure 4, n2) .

8. Claims 1-3,11-12,21-23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Emori et al. (U.S. Patent No. 6,314,017).

Regarding claim 1, Emori et al. disclose a two-transistor DRAM cell (Figure 1) consisting:

an NMOS device (Q1) with a first gate;

a PMOS device (Q2) with a second gate, the PMOS device coupled to the NMOS device (Figure 1, Q1 device coupled second gate of Q2 device at SN) ; and

a storage node coupled to the second gate (Figure 1, SN, **Column 9, lines 9-11, Figure 1 shown 2 of n-channel transistors, but one of transistors may also be configured as a p-channel transistor)** .

Regarding claim 2, Emori et al. disclose wherein the storage node is defined between the PMOS device and the NMOS device, the storage node having a voltage that converges to Vhigh, where Vhigh is greater than Vcc/2 (Column 7, lines 33-40, column 14, lines 24-35).

Regarding claim 3, Emori et al. disclose wherein the PMOS device (Figure 1, Q2) is coupled between the read bit line (RBL) and the read word line (RWL); and the NMOS device (Q1) is coupled to the PMOS device so as to define a storage node therebetween (Figure 1) **(Column 9, lines 9-11, Figure 1 shown 2 of n-channel transistors, but one of transistors may also be configured as a p-channel transistor)** .

Regarding claims 11-12, Emori et al. disclose a two-transistor DRAM cell (Figure 1) comprising:

a read bit line (RBL);

a write bit line (WBL);

a read word line (RWL);

a write word line (WWL);

a p-channel (PMOS) device (Q2) coupled between the read bit line and a read word line (figure 1) ; and an n-channel (NMOS) device (Q1) coupled between the write bit line and agate region of the PMOS device so as form a storage node therebetween (SN); **(Column 9, lines 9-11, Figure 1 shown 2 of n-channel transistors, but one of transistors may also be configured as a p-channel transistor).**

Regarding claim 17, Emori et al. disclose wherein a voltage level of storage node converges to logic high due to edge leakage current (Column 7, lines 53-67, Column 8, lines 1-16).

Regarding claim 21, Emori et al. discloses a system (Figure 1) comprising:

an integrated circuit (Figure 2); and

memory (Figure 2, MC) coupled to the IC, the memory including at least one two-transistor DRAM cell (Figure 21) consisting:

an NMOS device (Q1) with a first gate;

a PMOS device (Q2) with a second gate, the PMOS device coupled to the NMOS device (Figure 1, Q1 device coupled second gate of Q2 device at SN) ; and

a storage node coupled to the second gate (Figure 1, SN, **Column 9, lines 9-11, Figure 1 shown 2 of n-channel transistors, but one of transistors may also be configured as a p-channel transistor)** .

Regarding claims 22-23, Emori et al. disclose wherein the IC comprises a central processing unit (Figure2) , and at least one input/output module (Column 14, lines 12-15) coupled to the central processor unit and the memory is coupled to the IC via the communication channel (Figure 2, Column 22, lines 52-63, write operation and read operation came from a CPU).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

2/07/2006